

WHAT IS CLAIMED IS:

1. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference, said combination comprising:

5 a control processor comprising a means for ordering user signals; and
 a plurality of SIC-ATRF processors combining successive interface cancellation (SIC) multi-user detection and adaptive temporal reconstruction filtering in a successive arrangement wherein the output of one of the said processors is the input to the next successive processor, each of said SIC-ATRF processors comprising:
 a conventional detector;
 a respread processor;
 an adaptive temporal filter (ATRF); and
 a complex mathematical operation processor for canceling the reconstructed
 10 signal for the user from the total received signal.

15 2. The combination of claim 1 wherein each conventional detector is an IS-95 conventional detector comprising a short code despreader, a long code despreader, and a 64-ary matched filter bank.

 3. The combination of claim 1 wherein each conventional detector is an IS-95 rake conventional detector.

20 4. The combination of claim 1 wherein each ATRF comprises:
 tap weights;
 a tap delay line; and
 a mathematical summing circuit.

25 5. The combination of claim 4 wherein each SIC-ATRF processor further comprises a minimum cost channel estimate (MCCE) weight update processor.

 6. The combination of claim 4 wherein each ATRF further comprises a minimum cost channel estimate weight update processor.

 7. The combination of claim 4 wherein each ATRF is a minimum mean square error filter.

30 8. The combination of claim 1 wherein the output of each respread processor is the input for the ATRF.

 9. The combination of claim 8 wherein the input to each ATRF further comprises the outputs of the respread processors in all the previous SIC-ATRF processors.

10. The combination of claim 1 wherein each SIC-ATRF processor further comprises a frequency shift processor connected between the respread processor and the adaptive temporal filter.

11. The combination of claim 10 wherein each frequency shift processor comprises means to shift the frequency of the signal output from the respread processor to take into account Doppler spread.

12. A method in a combination system for enabling the receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a control processor and a plurality of SIC-ATRF processors in a successive arrangement, said method comprising:

ordering user signals according to a pre-defined methodology and assigning each user signal to one of the SIC-ATRF processors wherein each SIC-ATRF processor comprises a conventional detector, a respread processor, an adaptive temporal filter; and a complex mathematical operation processor for canceling the reconstructed signal for the user from the total received signal;

communicating a separate user code associated with the user signal to each SIC-ATRF processor according to the ordering;

in each successive SIC-ATRF processor, performing the steps of:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate;

estimating a channel for the user associated with the SIC-ATRF processor and reconstructing the signal interference associated with the user signal; and

canceling, in a mathematical operations processor, the reconstructed signal for the user associated with the SIC-ATRF processor from the total received signal.

if a plurality of SIC-ATRF processors remain, inputting the output of the current SIC-ATRF processor to the next successive SIC-ATRF processor.

13. The method of claim 12 wherein the step of ordering user signals according to a pre-defined methodology comprises ranking signals in descending order of received powers.

14. The method of claim 12 wherein the step of ordering user signals according to a pre-defined methodology comprises identifying signals above a certain threshold.

15. The method of claim 12 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and updating, in the ATRF, the filter tap weights.

16. The method of claim 15 wherein the pre-determined cost function is a minimum mean square error function.

17. The method of claim 12 wherein the channel estimation step further comprises: determining the adaptive filter tap weights by jointly minimizing the cost function between the received signal and the sum of the outputs of the respread processors of previous SIC-ATRF processors; and updating, in the ATRF, the filter tap weights.

18. The method of claim 17 wherein the pre-determined cost function is a minimum mean square error function.

19. A method in a combination system for enabling the receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a control processor and a plurality of SIC-ATRF processors in a successive arrangement, said method comprising:

ordering user signals according to a pre-defined methodology and assigning each user signal to one of the SIC-ATRF processors wherein each SIC-ATRF processor comprises a conventional detector, a respread processor, a frequency shift processor, an adaptive temporal filter; and a complex mathematical operation processor for canceling the reconstructed signal for the user from the total received signal.;

communicating a separate user code associated with the user signal to each SIC-ATRF processor according to the ordering;

in each successive SIC-ATRF processor, performing the steps of:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate;

shifting, in the frequency shift processor, the symbol estimate generated by the respread processor for the user associated with the SIC-ATRF processor;

estimating a channel for the user associated with the SIC-ATRF processor and reconstructing the signal interference associated with the user signal; and

canceling, in a mathematical operations processor, the reconstructed signal for the user associated with the SIC-ATRF processor from the total received signal.

If a plurality of SIC-ATRF processors remain, inputting the output of the current SIC-ATRF processor to the next successive SIC-ATRF processor.

20. The method of claim 19 wherein the channel estimation step further comprises:
determining the adaptive filter tap weights that minimize a pre-determined cost
5 function between the received signal and an output of the adaptive filter; and
updating, in the ATRF, the filter tap weights.

21. The method of claim 19 wherein the channel estimation step further comprises:
determining the adaptive filter tap weights by jointly minimizing the cost function
between the received frequency shift estimate and the sum of the outputs of the frequency
shift processors of previous SIC-ATRF processors; and
10 updating, in the ATRF, the filter tap weights.

22. In a wireless receiver for a CDMA system, a combination for enabling the
receiver to receive input signals at varied power levels in the presence of interference, said
combination comprising:

a plurality of processors in a parallel arrangement wherein the input to every
processor is a received signal, each of said parallel processors comprising:

- a conventional detector;
- a respread processor; and
- an adaptive temporal filter (ATRF); and

20 means for summing signals to form an interference estimate and subtracting the
estimate from the received signal.

23. The combination of claim 22 further comprising a control processor including a
means for ordering user signals.

24. The combination of claim 22 wherein the summation and subtraction means is a
series of mathematical operations processors.

25. The system of claim 22 wherein the summation and subtraction means is a
partial summer circuit.

26. The combination of claim 22 wherein each ATRF comprises:
tap weights;

- a tap delay line; and
- a mathematical summing circuit.

27. The combination of claim 26 wherein each parallel processor further comprises
an MCCE weight update processor.

28. The combination of claim 26 wherein each ATRF further comprises a minimum cost channel estimate weight update processor.

29. The combination of claim 22 wherein, in each parallel processor, the output of the respread processor is the input for the ATRF.

30. The combination of claim 22 wherein, in each parallel processor, the input to the ATRF comprises the outputs of the respread processors in all the other parallel processors.

31. The combination of claim 22 wherein each parallel processor further comprises a frequency shift processor connected between the respread processor and the ATRF.

32. The combination of claim 31 wherein each frequency shift processor comprises means to shift the frequency of the signal output from the respread processor to take into account doppler spread.

33. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference, said combination comprising:

a plurality of processors in a parallel arrangement wherein the input to every processor is a received signal, each of said parallel processors comprising:

a conventional detector; and

a respread processor;

an adaptive temporal filter (ATRF); and

means for summing signals to form an interference estimate and subtracting the estimate from the received signal.

34. The combination of claim 33 wherein the input to each ATRF comprises the outputs of the respread processors in all the parallel processors.

35. The combination of claim 33 wherein the ATRF further comprises a MCCE weight update processor.

36. The combination of claim 35 wherein each parallel processor further comprises a frequency shift processor connected between the respread processor in the parallel processor and the ATRF.

37. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a plurality of parallel processors and means for summing signals to form an interference estimate and subtracting the estimate from the received signal:

communicating a received signal to the plurality of parallel processors wherein each of the processors comprises a conventional detector, a respread processor, and an adaptive temporal filter (ATRF);

generating a reconstructed signal in each of the parallel processors for a user associated with the parallel processor; said generation step further comprising:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate; and

estimating a channel for the signal associated with the parallel processor and reconstructing the signal interference;

communicating the output of each parallel processor to a means for mathematically summing signals and subtracting signal estimates from the received signal;

generating, in the mathematical means, an interference estimate for each user; and

subtracting, in the mathematical means, the interference estimate from the received signal.

38. The method of claim 37 further comprising the steps of:

ordering user signals according to a pre-defined methodology; and

communicating a separate user code to a conventional detector in each parallel processor.

39. The method of claim 37 wherein the step of channel estimation step further comprises:

determining the adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

40. The method of claim 37 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights by jointly minimizing the cost function between the received signal and the sum of the outputs of the respread processors of all the other parallel processors; and

updating, in the ATRF, the filter tap weights.

41. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a plurality of parallel processors, an adaptive temporal filter (ATRF), and means for summing

signals to form an interference estimate and subtracting the estimate from the received signal, the method comprising the steps of:

communicating a received signal to the plurality of parallel processors wherein each of the processors comprises a conventional detector and a respread processor;

5 generating a reconstructed signal in each of the parallel processors for a user associated with the parallel processor; said generation step further comprising:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor; and

spreading, in the respread processor, the symbol estimate;

10 estimating a channel for the signal associated with each parallel processor and reconstructing the signal interference;

communicating the output of the ATRF to a means for mathematically summing signals and subtracting signal estimates from the received signal;

15 generating, in the mathematical means, an interference estimate for each user; and subtracting, in the mathematical means, the interference estimate from the received signal.

42. The method of claim 41 wherein the step of channel estimation step further comprises:

20 determining the adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

43. The method of claim 41 wherein the channel estimation step further comprises:

25 determining the adaptive filter tap weights by jointly minimizing the cost function between the received signal and the sum of the outputs of the respread processors of all the other parallel processors; and

updating, in the ATRF, the filter tap weights.

44. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a plurality of parallel processors and means for summing signals to form an interference estimate and subtracting the estimate from the received signal, the method comprising the steps of:

30

communicating a received signal to the plurality of parallel processors wherein each of the processors comprises a conventional detector, a respread processor, a frequency shift processor and an adaptive temporal filter (ATRF);

generating a reconstructed signal in each of the parallel processors for a user associated with the parallel processor; said generation step further comprising:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate;

shifting, in the frequency shift processor, the symbol estimate generated by the respread processor for the user association with the parallel processor; and

estimating a channel for the signal associated with the parallel processor and reconstructing the signal interference;

communicating the output of each parallel processor to a means for mathematically summing signals and subtracting signal estimates from the received signal;

generating, in the mathematical means, an interference estimate for each user; and subtracting, in the mathematical means, the interference estimate from the received signal.

45. The method of claim 44 wherein the step of channel estimation step further comprises:

determining the adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

46. The method of claim 44 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights by jointly minimizing the cost function between the received signal and the sum of the outputs of the respread processors of all the other parallel processors; and

updating, in the ATRF, the filter tap weights.

47. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference wherein said input signal is a vector comprised of one signal from each antenna in an antenna array of the receiver, said combination comprising:

a space-time adaptive processing (STAP) processor;

means for hypothesizing possible symbols transmitted during a symbol period;

a respread processor;

means for weight computation wherein the hypothesized symbol and the vector input symbol are used to form a set of STAP weights which filter the input data spatially and temporally;

5 a matched filter bank;

means for determining a metric to measure the quality of the matched filter bank; and
means for comparing generated metrics.

48. The combination of claim 47 wherein the STAP processor comprises a plurality of tapped delay lines, one per antenna element.

49. The combination of claim 47 wherein the possible symbols transmitted are the 64 Walsh symbols for an IS-95 reverse link transmitter.

50. The combination of claim 49 wherein the matched filter bank is a bank of 64 matched filters corresponding to the 64 Walsh symbols.

51. The combination of claim 47 wherein the means for weight computation further comprises a means for using previously detected or known symbols.

52. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said input signal is a vector comprised of one signal from each antenna in an antenna array of the receiver; the method comprising the steps of:

receiving the input signal vector;

determining a metric, said determining step comprising:

hypothesizing which symbol was transmitted;

respreading the hypothesized symbol;

determining STAP weight update based on respread hypothesized symbol and

input signal vector;

applying a tap delay line to each signal vector component;

applying STAP weights to each signal vector component, one per antenna;

summing the weighted results in a mathematical summation circuit;

despreading the output of the summation circuit and inputting the despread

signal to a matched filter bank; and

generating a metric associated with the hypothesized signal;

repeating the metric determining step for each of the possible 64 Walsh symbols;

comparing each of the 64 metrics; and

determining, based on the comparison, the transmitted symbol.

53. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said input signal is a vector comprised of one signal from each antenna in an antenna array of the receiver; the method

comprising the steps of:

receiving the input signal vector;

determining a metric, said determining step comprising:

hypothesizing which symbol was transmitted;

respreading the hypothesized symbol;

determining STAP weight update based on respread hypothesized symbol and input signal vector;

despreading the delayed signal vector components, one per antenna;

applying the STAP weights to each of the despread signal vector components;

summing the weighted results in a mathematical summation circuit; and

generating a metric associated with the hypothesized signal;

repeating the metric determining step for each of the possible 64 Walsh symbols;

comparing each of the 64 metrics; and

determining, based on the comparison, the transmitted symbol.

54. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference wherein said input signal is a vector comprised of one signal from each antenna in an antenna array of the receiver, said combination comprising:

a control processor comprising a means for ordering user signals; and

a plurality of STAP/VSIC-ATRF processors combining successive interface cancellation (SIC) multi-user detection, space-time adaptive processing and adaptive temporal reconstruction filtering in a successive arrangement wherein the output of one of the said processors is the vector input to the next successive processor, each of said STAP/VSIC-ATRF processors comprising:

a space-time adaptive processing (STAP) processor;

a plurality of adaptive temporal filters (ATRFs), one per antenna; and

a plurality of complex mathematical operation processors, one per ATRF, for canceling the reconstructed signal for the user from the total received signal.

55. The combination of claim 54 wherein each STAP processor comprises:

a plurality of filters, one per antenna;

a mathematical summation processor for combining the outputs of all the filters;
 a conventional detector; and
 a minimum cost channel weight update processor.

56. The combination of claim 55 wherein the STAP processor is a blind adaptive

5 STAP processor.

57. The combination of claim 55 wherein each STAP/VSIC-ATRF processor further comprises a plurality of respread processors.

58. The combination of claim 55 wherein each STAP processor further comprises a respread processor.

59. The combination of claim 54 wherein each ATRF comprises:

tap weights;

a tap delay line; and

a mathematical summing circuit.

60. The combination of claim 59 wherein each ATRF further comprises a minimum cost channel estimate weight update processor.

61. The combination of claim 57 wherein, in each STAP/VSIC-ATRF processor, the output of the respread processor is the input for the plurality of ATRFs.

62. The combination of claim 57 wherein, in each STAP/VSIC-ATRF processor, the input to the plurality of ATRFs further comprises the outputs of the respread processors in all the previous STAP/VSIC-ATRF processors.

63. The combination of claim 57 wherein each STAP/VSIC-ATRF processor further comprises a plurality of frequency shift processors connected between the respread processor and the plurality of ATRFs.

64. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference, said combination comprising:

a plurality of processors in a parallel arrangement wherein the input to every processor is a received signal, each of said parallel processors comprising:

a space-time adaptive processing (STAP) processor; and

a plurality of adaptive temporal filters (ATRFs); and

means for summing signals to form an interference estimate and subtracting the estimate from the received signal.

65. The combination of claim 64 wherein each STAP processor comprises:

a plurality of filters, one per antenna;

a mathematical summation processor for combining the outputs of all the filters; and a conventional detector.

66. The combination of claim 64 wherein each parallel processor further comprises an MCCE weight update processor.

67. The combination of claim 65 wherein each STAP processor further comprises an MCCE weight update processor.

68. The combination of claim 64 wherein each parallel processor further comprises a of respread processor.

69. The combination of claim 65 wherein each STAP processor further comprises a respread processor.

70. The combination of claim 64 wherein the summation and subtraction means is a series of mathematical operations processors.

71. The combination of claim 64 wherein the summation and subtraction means is a series of mathematical operations processors.

72. The combination of claim 64 wherein each ATRF comprises:
tap weights;
a tap delay line; and
a mathematical summing circuit.

73. The combination of claim 68 wherein, in each parallel processor, the output of the respread processor is the input for the plurality of ATRFs.

74. The combination of claim 68 wherein, in each parallel processor, the input to the plurality of ATRFs further comprises the outputs of the respread processors in all the other parallel processors.

75. The combination of claim 68 wherein each parallel processor further comprises a plurality of frequency shift processors connected between the respread processor and the plurality of ATRFs.